AN INVESTIGATION INTO THE DEVELOPMENT OF TIN-LEAD AND LEAD-FREE SOLDER PASTES TO REDUCE VOIDING IN LARGE CONTACT AREA POWER TRANSISTOR/ QFN TYPE COMPONENTS

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ABSTRACT
Over the last few years, there has been an increase in the use of component parts such as QFNs and Power Transistors which have large solder paste contact areas underneath the component. Voiding has been found to be drastically increased with these large contact area components compared with typical BGA/CSP components. This has been the result of the larger solder paste volumes applied underneath the part together with the difficulty of the low boiling point flux gases to escape from under the part during reflow soldering.

Various techniques have been employed to reduce the voiding by reducing the amount of solder paste printed under the large contact area component parts as well as reflow profile development. This has reduced the amount of voiding somewhat but the voiding has still been sufficient in some cases to give concerns in terms of thermal heat dissipation and reliability requirements for these soldered components on the board.

This study was done to investigate different flux activators systems which had higher heat resistivity and activation levels over the melting point of the tin-lead and lead-free solders tested. Test vehicles were assembled using different tin-lead and lead-free solder paste flux formulations with power transistor components on different board surface finishes (OSP, NiAu, Sn, SnAgCu HASL) to assess the amount of voiding present after reflow. The results of the investigations will be presented.

Key words: Lead-free, Tin-lead, Voiding, Power Transistor, QFN, Reflow

INTRODUCTION

Voiding especially in large contact area solder joints is problematic because it could not only affect reliability, but it can also deteriorate the thermal heat dissipation properties which could lead to component failure.

For voiding of BGA/CSP components voiding is less than 25% of the area [1] but for components such as power transistors/QFN there is no criteria provided. Generally for the large center pad the typical voiding criteria would be less than 50% but if there is a thermal or electrical requirement, the voiding percentage would be more critical which could affect the component reliability. There have been limited studies in this area to determine what the voiding percentage would be to give an electrical and thermally reliable solder joint for the large center pad. One study indicated that for these types of components with 30% voiding there was no deterioration in electrical or thermal properties during reliability testing [2]. The voiding percentage in the center pad would be dependent on many factors such as the thermal via designs in the center pad, the stencil aperture design affecting solder paste volume, the reflow profile and atmosphere and the type of solder paste used [3, 4].

The following shows a common mechanism of occurrence of voids under the larger solder paste contact area parts:

1. In the pre-heat stage of the reflow profile, the flux medium in the paste softens and starts to bleed out from the solder paste. The component solderable surface and board pads are similarly oxidized.

2. The solder then melts in the reflow profile stage and water vapor is formed by the reaction between the organic acids of the flux and the oxides from the solder metal. Low boiling point materials, such as flux additives and rosins are converted into gases.

3. In such cases where some of the low boiling point materials remain at the reflow stage, they continue to outgas for some time and may be entrapped beneath the component in the solder joint creating voids in the solder joint on cooling.

The steps in the formation of voids under larger solder pasted components is shown in Figure 1.

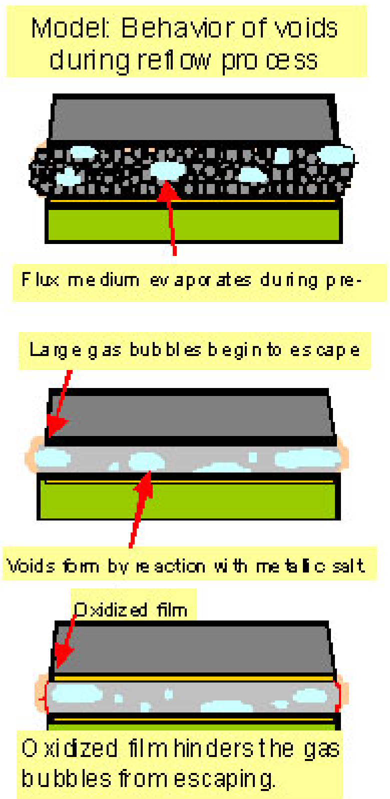

Figure 1: Mechanism of voiding formation under large contact area components during the reflow process.

The objective of this work was an assessment and development of tin-lead and lead-free solder paste developed to produce low voiding during reflow on large solder paste contact areas underneath components such as Power Transistors and QFNs which is described in the following sections.

EXPERIMENTAL

Tin-Lead Solder Paste Evaluations

For the no-clean tin-lead paste evaluation, two Type 3 solder pastes were tested. These were Tin-lead Paste A which had adjustments in the flux formulation to try and reduce voiding and Conventional Tin-lead Paste B which was used as the baseline tin-lead solder paste.

An internally company developed test board was used with OSP board surface finish with power transistor, 1mm pitch CSP and 6330 [2512] chip components on the board. The stencil thickness used during paste printing of the board was 120µm (5 mils).

The stencil apertures for the power transistor, CSP and 6330 components were 1:1 with the board pad apart from the power transistor component which had the stencil apertures as shown in Figure 2. The stencil apertures were the same for tin-lead Paste A and B. Paste was printed on certain test boards at time zero and on certain test boards after the paste had been conditioned with 8 hours of solder paste rolling on a stencil.

Figure 2: Stencil apertures used for the power transistor component.

The reflow oven used was a convection type with reflow in an air atmosphere. The reflow profile was used was as shown in Figure 3 with the same profile used for tin-lead paste A and B. The peak temperature was 215°C, with time over 183°C of around 50 seconds and preheat time between 140°C to 160°C of 90 seconds. The component finish for the power transistor and 6330 [2512] chip component was Sn90Pb10. The CSP sphere alloy composition was Sn40Pb.

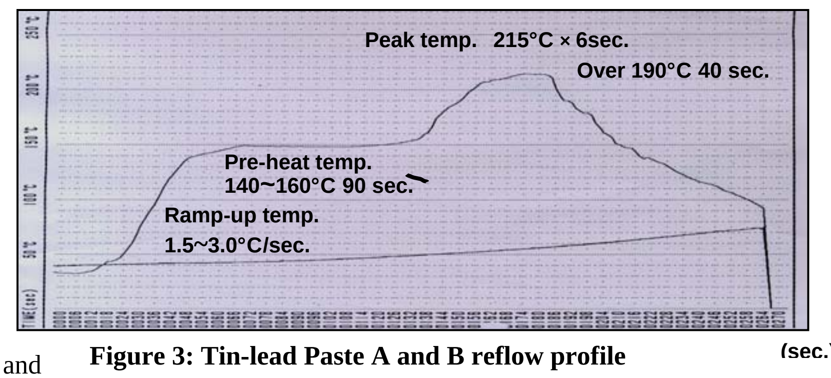

Figure 3: Tin-lead Paste A and B reflow profile

Lead-Free Solder Paste Evaluations

For the lead-free Sn3Ag0.5Cu no-clean paste evaluation, two Type 3 solder pastes were tested. These were Lead-free Paste C which had adjustments in the flux formulation to try and reduce voiding and Conventional Lead-free Paste D which was used as the baseline lead-free solder paste. The test board used was evaluated with four board surface finishes which were OSP, NiAu, Sn, Sn3Ag0.5Cu HASL which used the same test board design as for the tin-lead paste evaluation.

The stencil thickness used during paste printing was 120µm (5 mils) with the same stencil apertures for the power transistor as used in the tin-lead paste evaluation which was the only component evaluated on the lead-free test board. The component finish for the power transistor was pure tin.

The reflow oven was a convection type with reflow in an air atmosphere. The reflow profile used had a peak temp. of 238°C, with time over 217°C of 50 sec. The preheat time between 150°C and 190°C was 110 sec. The reflow profile is shown in Figure 4. The same reflow profile was used for conventional lead-free Paste D as lead-free Paste C.

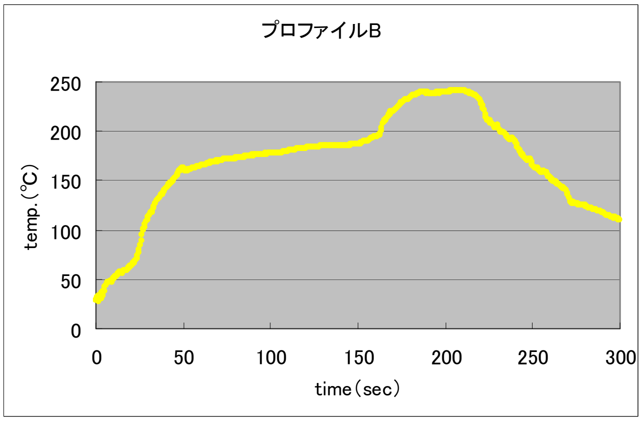

Figure 4: Lead-free reflow profile

RESULTS AND DISCUSSION

Tin-Lead Solder Paste Evaluation

The flux activator systems used in the newer tin-lead and lead-free paste evaluations were found to give a reduction in voids at the joints of the large contact area components especially for lead-free soldering.

These solder paste fluxes were found to improve the removal of oxidized films on the solder surface and enhance the removal of the flux gases generated. The specific flux activators also retained good wetting properties with a larger pull force on the component, making it easier for the flux gases to be pushed out from under the part.

The X-ray images for Tin-lead Paste A after reflow for the initial time zero test boards and after 8 hours solder paste rolling on the stencil are shown in Figures 5 and 6.

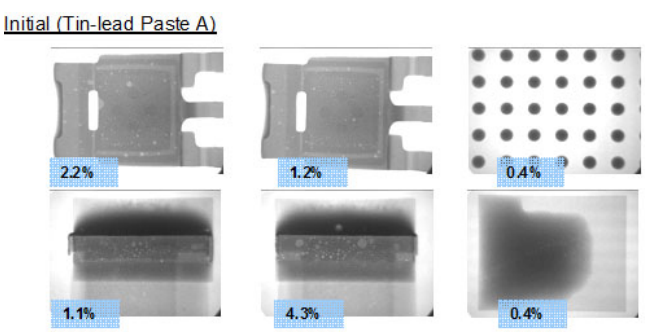

Figure 5: X-ray images of Paste A after reflow at Time zero (Top row: 2 power transistors and CSP component; Bottom row: 6330[2512] chip component terminations and unpopulated power transistor board location)

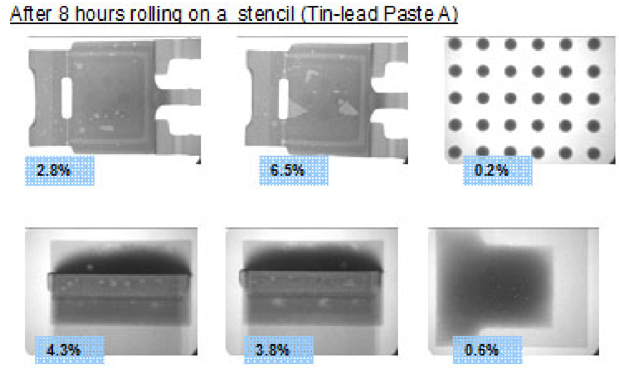

Figure 6: X-ray images of Paste A after reflow after 8 hours of solder paste rolling on a stencil (Top row: 2 power transistors and CSP component; Bottom row: 6330[2512] chip component terminations and unpopulated power transistor board location).

For Paste A the voiding ranged from 0.2% up to 6.5% across all components which is relatively low. For the power transistor component the voiding ranged from 1.2% to 2.2% during initial time zero printing with an increase from 2.8% to 6.5% after 8 hours of paste rolling on a stencil.

The X-ray images for Conventional Tin-lead Paste B after reflow for the initial time zero test boards and after 8 hours paste rolling on the stencil are shown in Figures 7 and 8.

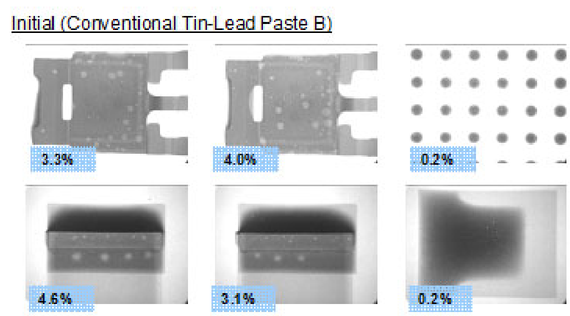

Figure 7: X-ray images of Paste B after reflow at Time zero (Top row: 2 power transistors and CSP component; Bottom row: 6330[2512] chip component terminations and unpopulated power transistor board location).

After 8 hours rolling on a stencil (Conventional tin-lead Paste B)

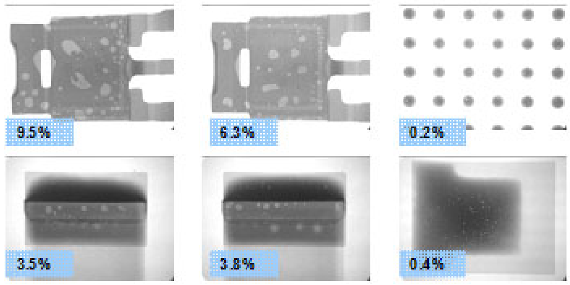

Figure 8: X-ray images of Paste B after reflow after 8 hours of solder paste rolling on a stencil (Top row: 2 power transistors and CSP component; Bottom row: 6330[2512] chip component terminations and unpopulated power transistor board location).

For Paste B the voiding ranged from 0.2% up to 9.5% across all components. For the power transistor components the voiding ranged from 3.3% to 4% during initial time zero printing with an increase from 6.3% to 9.5% after 8 hours of paste rolling on a stencil. This was a higher voiding percentage with the power transistor than compared with Tin-lead paste A as shown in Table 1 which indicates the improved voiding performance with Tin-lead paste A.

	Initial	After 8 hours paste rolling
Tin-Lead Paste A	1.2 to 2.2%	2.8 to 6.5%
Tin-Lead Paste B	3.3 to 4%	6.3 to 9.5%

Table 1: Power Transistor voiding comparison between Tin-Lead Paste A and Paste B for Time zero boards and after 8 hours paste rolling on the stencil.

Although there was a decrease in voiding from Tin-lead Paste B to Tin-lead Paste A, the actual voiding percentage was not very large potentially due to the improved wetting of tin-lead solder.

Lead-Free Solder Paste Evaluation

The results for Lead-free SnAgCu paste C for the power transistor on a range of board surface finishes is shown in Figure 9.

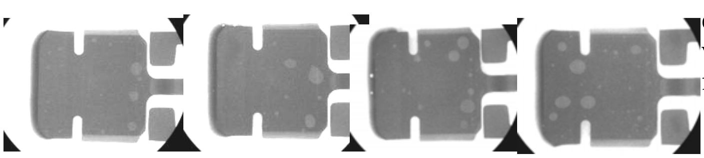

Figure 9: Lead-free Paste C voiding data on the power transistor assembled on different board surface finishes (OSP [2.6% voiding], Pure tin [3.6% voiding], NiAu [5.4% voiding], Sn3Ag0.5Cu HASL[4.6% voiding]).

The results for the conventional lead-free SnAgCu paste D for the power transistor on a range of board surface finishes is shown in Figure 10.

Figure 10: Conventional Lead-free Paste D voiding data on the power transistor assembled on different board surface finishes (OSP [25.2% voiding], Pure tin [35% voiding], NiAu [17.5% voiding], Sn3Ag0.5Cu HASL [17.4% voiding]).

Voiding was drastically reduced with large contact area components, regardless of the type of surface finish used comparing Lead-free Paste C (Figure 9) with Conventional Lead-free Paste D (Figure 10). Voiding with Paste C varied from 2.6% to 5.4%. Voiding with Paste D varied from 17.4% to 35%. These results are shown in Table 2.

	OSP	Pure Sn	NiAu	Sn3Ag0.5Cu HASL
Lead-free Paste C	2.6%	3.6%	5.4%	4.6%
Lead-free Paste D	25.2%	35%	17.5%	17.4%

Table 2: Power Transistor voiding comparison between Lead-free Paste C and Paste D for the four different board surface finishes (OSP, Pure Sn, NiAu, Sn3Ag0.5Cu HASL).

Based on the results in Table 2, a significant overall reduction can be seen in voiding with lead-free Paste C versus Lead-free Paste D.

Lead-free Paste C, was designed to reduce voiding with the difference in voiding across all the board surface finishes small. In certain cases pure tin board surface finish may have increased voiding as shown in Table 2 for Lead-free Paste D.

Lead-free Paste C used a new halogen-free activator system and it was found to be successful in reducing the occurrence of voids. The mechanism for reducing the voiding for Lead-free Paste C would be as mentioned in the following steps:

1. Prior to reaching the peak reflow zone, evaporation of low boiling point materials would generate gases (this would also be the case for the conventional lead-free solder paste D).

2. At the peak reflow zone, the newly developed activator in Paste C would start to react. As the activator in Paste C had a high heat resistivity than that for Paste D, and could retain high activation levels even over the Sn3Ag0.5Cu

melting point (217ºC), the activator would continue to be available to remove oxidized film on the solder surface and maintain the flow of flux, prompting the increased removal of flux gases from the solder joint for Paste C.

3. The activator would also retain good wetting properties and a large pull force, making it even easier for the gases to escape for Paste C. As a result, it would enable a significant reduction in voids at the joint of large contact area components such as power transistor/ QFN components which is shown in Figure 11.

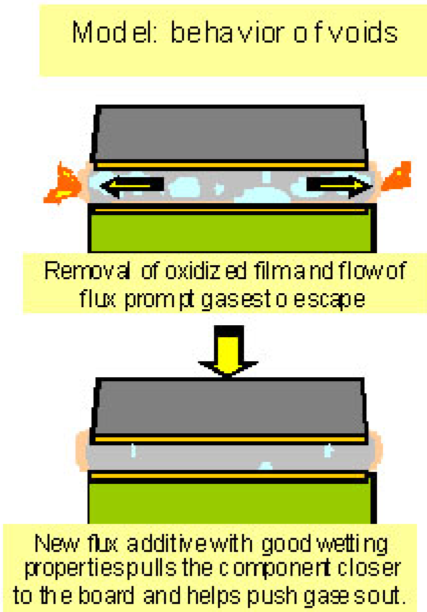

Figure 11: Movement of voids during the reflow process for lead-free Paste C

The improved wetting property for Lead-free Paste C would also extend the duration of the fluid/active state of the flux, and help to push out more of the entrapped gas from the molten solder paste, enabling the component to come closer to the board pad and lowering the component solder joint standoff height.

The Lead-free Type 3 paste C also had good durability in continuous printing without any degradation in reflow evaluations over time based on the type of flux developed as shown in Figure 12.

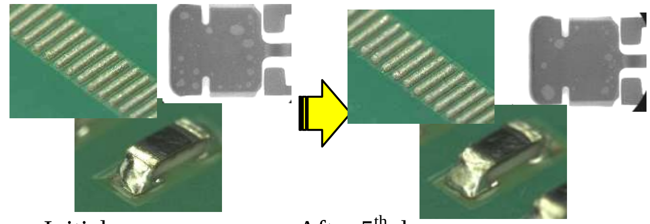

Figure 12: Printing and reflow performance of Lead-free Paste C after initial paste printing and reflow and after paste printing and reflow trials over a period of five days.

Additives used in Lead-free Paste C do not react at room temperature, so the flux reaction with the solder powder at room temperature would be kept to a minimum. The solder paste also had consistent quality and performance over the period of five days which was also confirmed in paste viscosity and thixotropic index studies.

CONCLUSIONS

During the development of tin-lead solder paste, the changes in flux formulation were found to reduce the voiding in Tin-lead Paste A compared with conventional paste B on large surface contact power transistor components.

The affect of improving flux formulation was also found to a greater extent for Lead-free paste C compared with conventional lead-free paste D during reflow studies on power transistor components. The lead-free paste C successfully reduced voiding with a newly adopted flux activator.

The difference in voiding behavior among tin-lead solder pastes would typically be smaller than that of lead-free solder pastes because the tin-lead alloy has good wetting characteristics which help reduce voiding and make it less dependent on the flux formulation.

For Lead-free Paste C, a significant reduction in voids at the joint of large contact area components such as power transistor/ QFN components was achieved compared with Lead-free Paste D. This was due to the flux activator used in Lead-free Paste C which had a high heat resistivity that that for Lead-free Paste D, and could retain higher activation levels even over the Sn3Ag0.5Cu melting point

The flux activator would continue to be available to remove oxidized film on the solder surface and maintain the flow of flux, prompting the removal of flux gases from the solder joint. The activator would also help to retain good wetting properties and a large pull force between the component and board, making it even easier for the gases to escape the solder joint.

By enabling the removal of voids from large contact area components, thermal heat dissipation properties would be enhanced.

FUTURE WORK

Work was currently under way to reduce the voiding to a greater extent for new tin-lead and lead-free pastes under development.

ACKNOWLEDGEMENTS

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REFERENCES

1. IPC-A-610 standard, Acceptability of Electronic Assemblies, 2010.
2. International Rectifier Application Note An-1133 (PQFN), April 2010.
3. A. Syed et al., Board Design, Surface Mount Assembly and Board Level Reliability Aspects of FusionQuad packages, SMTAI conference, 2008.
4. S. Sethuraman et al., Board Level Assembly and Rework Assessment of Thin Substrate Chip Scale Package (tsCSP), a Multi-Row Leadless Package, 40^{th} International Symposium on Microelectronics (IMAPS), 2007.